3/08/05 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Steven Harold SLUPSKY
Serial no.	:	10/666,553
Filed	:	September 19, 2003
For	:	NON-CONTACT TESTER FOR ELECTRONIC CIRCUITS
Group Art Unit	:	2829
Examiner	:	Jimmy NGUYEN
Docket	:	THOLAM P212US

The Commissioner for Patents
U.S. Patent & Trademark Office
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Alexandria, VA 22313-1450

SUBMISSION OF CERTIFIED COPY

Dear Sir:

A claim for priority is hereby made under the provisions of 35 U.S.C. § 119 for the above-identified United States Patent Application based upon Canadian Patent Application No. 2,404,183 filed September 19, 2002. A certified copy of said Canadian application is enclosed herewith.

In the event that there are any fee deficiencies or additional fees are payable, please charge the same or credit any overpayment to our Deposit Account (Account No. 04-0213).

Respectfully submitted,

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This is to certify that the documents attached hereto and identified below are true copies of the documents on file in the Patent Office.

Specification and Drawings, as originally filed, with Application for Patent Serial No: **2,404,183**, on September 19, 2002, by **SCANIMETRICS INC.**, assignee of Steven Harold Slupsky, for "Non-Contact Tester for Integrated Circuits".

Agent certificateur/Certifying Officer

January 10, 2005
Date

Canada

OPIC CIPO

ABSTRACT OF THE DISCLOSURE

A non-contact tester for integrated circuits consists of an integrated circuit and independent scanning head, in combination. The integrated circuit includes a micro-fabricated wireless contact and means for sending and receiving signals via the wireless contact. The independent scanning head has a wireless contact compatible with the wireless contact on the integrated circuit. This enables data to be exchanged with the integrated circuit to confirm proper functioning of the integrated circuit.

TITLE OF THE INVENTION:

Non-Contact Tester For Integrated Circuits

FIELD OF THE INVENTION

The present invention relates to testers for integrated circuits

BACKGROUND OF THE INVENTION

Integrated circuits must be tested to ensure that they are not defective. At the present time this is done through the use of mechanical probes. The mechanical probes touch down on the integrated circuit and data is passed through the circuit. However, in making contact with the integrated circuit damages sometimes occurs when the mechanical probes make physical contact.

SUMMARY OF THE INVENTION

What is required is a tester for integrated circuits which is able to test the integrated circuits without making physical contact.

According to the present invention there is provided a non-contact tester for integrated circuits which consists of an integrated circuit and independent scanning head, in combination. The integrated circuit includes a micro-fabricated wireless contact and means for sending and receiving signals via the wireless contact. The independent scanning head has a wireless contact compatible with the wireless contact on the integrated circuit. This enables data to be exchanged with the integrated circuit to confirm proper functioning of the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings, the drawings are

for the purpose of illustration only and are not intended to in any way limit the scope of the invention to the particular embodiment or embodiments shown, wherein:

FIGURE 1 is a top plan view of an integrated circuit fabricated in accordance with the teachings of the present invention.

FIGURE 2 is a representation of an independent scanning head scanning a series of integrated circuits in accordance with the teachings of the present invention.

FIGURE 3 is a top plan view of a test circuit.

FIGURE 4 is an enlarged top plan view of the test circuit illustrated in **FIGURE 3**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment, a non-contact tester for integrated circuits will now be described with reference to **FIGURES 1** through 4.

This non-contact tester is comprised of a silicon substrate and a plurality of microfabricated antennae structures. Each antenna is located within the silicon substrate in a manner such that when the scanning antenna is aligned with the DUT on a wafer, each antenna is coincident in 2 dimensions to a reciprocal antenna structure located on the DUT.

Power is coupled to the wafer by way of microfabricated MEMS cantilever test probes. Alternatively, power may be coupled using RF energy by way of microfabricated antennae structures patterned on the same substrate as the Virtual Probe structures. Alternatively, power may be coupled magnetically using microfabricated inductors or transformers. Alternatively, power may be coupled optically by way of incident laser energy on a microfabricated structure on the DUT.

The Virtual Probe Card comprises of a microfabricated scanning antenna, a printed circuit board and a plurality of electronic circuits.

Frequency discrimination between adjacent pads is by way of different oscillating frequencies. This is accomplished using ring oscillator chains of different length.

Antenna size and structure on the wafer is matched to the ring oscillator frequency.

The scanning circuits located in the scanning head "auto tune" to the carrier frequency of the test circuit transmitter located on the wafer. Encoded data is received and decoded from the carrier signal.

A simple rectifier circuit is used to decode the signal transmitted from the scanning head to the wafer.

Test vectors may be generated "on chip" using BIST techniques. Alternatively, test vectors may be generated using a memory element and logic sequencer.

Test vectors may be generated externally and coupled to the DUT using the scanning head. Test vectors may be applied to individual i/o pads in this way.

The present invention comprises a test circuit for testing an integrated circuit on a wafer during wafer test (Functional test).

The present invention comprises a test circuit for testing an integrated circuit on a wafer during wafer fabrication (Process Control Monitoring).

Antenna structures are approximately the same size as

standard bond pads.

Optionally, optical methods may be used to interface to the integrated circuit. High speed CMOS image sensors and high speed PIN diodes.

Optionally, magnetic methods may be used to interface to the integrated circuit. High speed Giant Magneto Resistive Thin Film heads and high speed magnetic coils.

This technology allows for testing integrated circuits during the IC fabrication process using wireless RF telemetry. The technology adds to or replaces existing bonding pads in an integrated circuit with an RF transceiver device. This device can act as a bonding pad during manufacture and test of an integrated circuit and communicates information in a wireless manner. Using this virtual Test Probe, semiconductor manufacturers can stop the trend of growing test costs with respect to transistor fabrication cost while at the same time improving test performance in areas that are causing very serious problems.

The solution saves money in several ways at the same time;

1. Virtual Test Probes are significantly less expensive than current mechanical probe cards.
2. Virtual Probes eliminate i/o bond pad damage during touch downs.
3. Mechanical probes cards "wear out" due to mechanical failure. Virtual Test Probes do not suffer from mechanical wear and therefore require less cleaning and maintenance.
4. Virtual Test Probes offer unique prototype test capabilities not available with conventional test methods such as internal test points.

5. Virtual Test Probes can test to smaller geometries and at higher speeds, thereby postponing expensive test equipment upgrades.
6. The Virtual Probe technology provides improved test coverage by allowing the integrated circuit to be tested "at speed".

In this patent document, the word "comprising" is used in its non-limiting sense to mean that items following the word are included, but items not specifically mentioned are not excluded. A reference to an element by the indefinite article "a" does not exclude the possibility that more than one of the element is present, unless the context clearly requires that there be one and only one of the elements.

It will be apparent to one skilled in the art that modifications may be made to the illustrated embodiment without departing from the spirit and scope of the invention as hereinafter defined in the Claims.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A non-contact tester for integrated circuits, comprising in combination:

an integrated circuit which includes a micro-fabricated a wireless contact and means for sending and receiving signals via the wireless contact;

an independent scanning head having a wireless contact compatible with the wireless contact on the integrated circuit, such that data may be exchanged with the integrated circuit to confirm proper functioning of the integrated circuit.

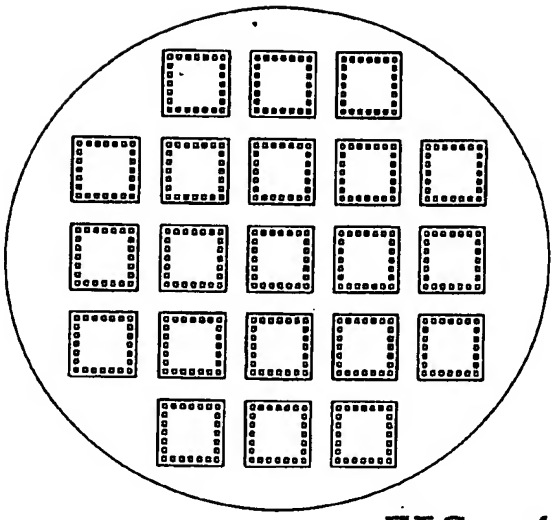

FIG. 4

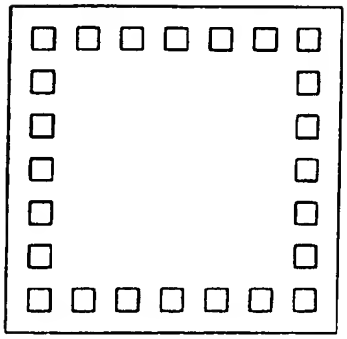

FIG. 3

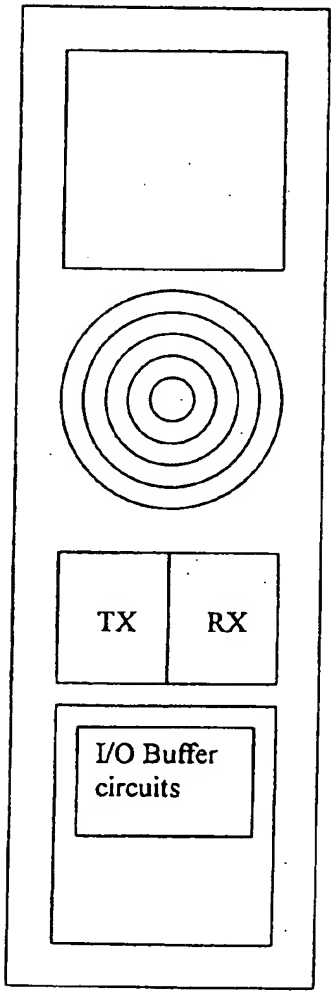

FIG. 1

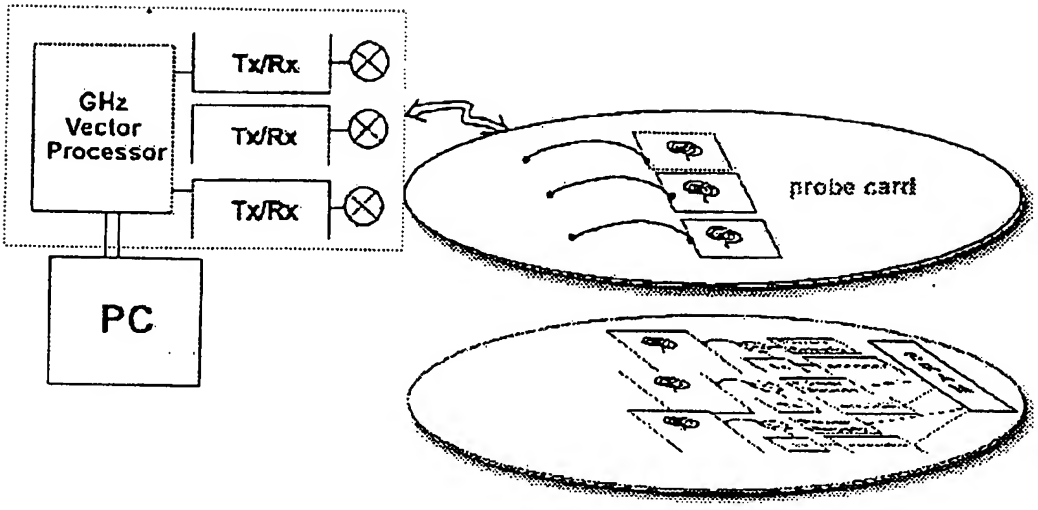

FIG. 2